

Notice of References Cited

Application/Control No.

09/677,913

Applicant(s)/Patent Under
Reexamination
DITLOW ET AL.

Examiner

Samuel Broda

Art Unit

2123

Page 1 of 2

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,225,143 B1	05-2001	Rao et al.	438/106
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
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	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Buffet et al, "Methodology for I/O Cell Placement and Checking in ASIC Designs Using Area-Array Power Grid," Proceedings of the IEEE 2000 Custom Integrated Circuits Conference, pp. 125-128 (May 2000)
	V	Hayashi et al, "EMI-Noise Analysis Under ASIC Design Environment," ACM Proceedings of the 1999 International Symposium on Physical Design, pp. 16-21 (September 1999)
	W	Kar et al, "Optimizing C4 Bump Placements for a Peripheral I/O Design," 1999 IEEE Proceedings of the 49th Conference on Electric Components and Technology, pp. 250-254 (June 1999)
	X	Caldwell et al, "Implications of Area-Array I/O for Row-Based Placement Methodology," 1998 IEEE Symposium on IC/Package Design Integration, pp. 93-98 (February 1998)

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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	U	Farbarik et al, "CAD Tools for Area Distributed I/O Pad Packaging," 1997 IEEE Multi-Chip Module Conference, pp. 125-129 (February 1997)
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